# Heterogeneous Integration of Enhancement Mode $In_{0.7}Ga_{0.3}As$ Quantum Well Transistor on Silicon Substrate using Thin (≤ 2 μm) Composite Buffer Architecture for High-Speed and Low-voltage ( 0.5V) Logic Applications

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## Abstract

This paper describes for the first time, the heterogeneous integration of $In_{0.7}Ga_{0.3}As$ quantum well device structure on Si substrate through a novel, thin composite metamorphic buffer architecture with the total composite buffer thickness successfully scaled down to 1.3μm, resulting in high-performance short-channel enhancement-mode $In_{0.7}Ga_{0.3}As$ QWFETs on Si substrate for future high-speed digital logic applications at low supply voltage such as 0.5V.

## Introduction

The InGaAs quantum well field effect transistor (QWFET) is one of the most promising device candidates for future high-speed and low-power digital logic applications due to high electron mobility, large Γ to L valley separation and good short-channel performance [1-3]. A seamless, robust heterogeneous integration of high-performance InGaAs QWFET on Si substrate will allow low-voltage, high-speed III-V based logic circuit blocks to couple with the main stream Si CMOS platform for future microprocessor applications, while avoiding the need for developing large diameter (≥300mm) III-V substrates. This paper describes in detail for the first time, the integration of $In_{0.7}Ga_{0.3}As$ quantum well (QW) structure on Si through a novel, thin composite metamorphic buffer architecture consisting of GaAs and graded $In_xAl_{1-x}As$ layers, resulting in short-channel enhancement-mode $In_{0.7}Ga_{0.3}As$ QWFETs on silicon with high performance at low supply voltage of 0.5V.

## Materials Growth and Characterization

$In_{0.7}Ga_{0.3}As$ quantum well (QW) device layers shown in Fig. 1 were heterogeneously grown on $4^o$ off-cut (100) p-type Si substrates with lattice mismatch of >8% using a composite metamorphic buffer consisting of GaAs and graded $In_xAl_{1-x}As$ layers by solid source MBE. The thickness of the composite buffer is successfully scaled down to 1.3μm for the first time without degrading the properties of $In_{0.7}Ga_{0.3}As$ QW. Figs. 2a-2b show cross-sectional TEM images of the entire structure grown on Si with 1.5μm and 1.3μm composite buffer, respectively. In both cases, the misfit and threading dislocations are predominantly contained in the composite buffer, and the active device layers are virtually defect-free, which is also shown in Fig. 2c using high-resolution TEM. The relaxation state and the grading scheme were evaluated using high-resolution x-ray rocking curve, as shown in Fig. 3. The angular separation between the diffraction peaks of GaAs with respect to Si confirms full relaxation of the GaAs layer. The indium composition of the $In_xAl_{1-x}As$ buffer layer is graded from 0 to 52%, with an overshoot of indium concentration (0.52<x<0.7) in-between, as evidenced by the two peaks existing in the $In_xAl_{1-x}As$ buffer region of Fig. 3. This overshoot was employed to ensure full relaxation of this buffer layer while minimizing its total thickness. The relaxation of the entire composite buffer layer allows the growth of a defect-free $In_{0.7}Ga_{0.3}As$ QW on Si (Figs.2a-2c). Figs. 2c and 3 suggest the $In_{0.7}Ga_{0.3}As$ QW layer is compressively strained with respect to the $In_{0.52}Al_{0.48}As$ barrier. AFM surface morphology of the $In_{0.7}Ga_{0.3}As$ QW layers grown on Si with 2μm and 1.3μm composite buffers exhibit a cross-hatch pattern, as shown in Figs. 4a and 4b respectively, demonstrating excellent metamorphic growth of the buffer layers. The surface *rms* roughness of $In_{0.7}Ga_{0.3}As$ QW grown on Si was measured over an area of $5x5\mu m^2$ to be less than 4nm, which is similar to that of $In_{0.7}Ga_{0.3}As$ QW grown on GaAs [4].

Figure 5a shows the $In_{0.7}Ga_{0.3}As$ QW mobility at 300K and 77K as a function of total buffer thickness ranging from 3.2μm to 1.3μm of the composite buffer grown on Si. No mobility degradation is observed for all the buffer thicknesses, demonstrating that the thin composite metamorphic buffer architecture is effective in filtering dislocations. Fig. 5b compares the Hall mobility versus sheet carrier density (Ns) measured in the $In_{0.7}Ga_{0.3}As$ QW layers grown on Si, GaAs and InP substrates at 300K and 77K. For a given Ns, the mobility in the $In_{0.7}Ga_{0.3}As$ QW layer grown on silicon via the composite buffer is equivalent to those in the $In_{0.7}Ga_{0.3}As$ QW layers grown on III-V substrates such as GaAs and InP. No degradation in QW mobility on Si is observed despite the >8% lattice mismatch, demonstrating effective dislocation filtering using the composite buffer on Si. Fig. 6a shows the quantitative mobility spectrum analysis (QMSA) for $In_{0.7}Ga_{0.3}As$ QW on Si at different temperatures. The large conductivity ratio between the majority carrier (electrons) and the minority carrier (holes) at all temperatures and also the increase in electron mobility with decreasing temperature suggest no parallel, parasitic conduction in Si or through the composite buffer layer. In addition, both Ns and mobility exhibit no dependence on magnetic field at different

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temperatures, as shown in Fig. 6b, further indicating no parallel, parasitic conduction in the buffer layer or in Si.

## Device Characteristics

Figure 7 shows the SEM micrograph of an $In_{0.7}Ga_{0.3}As$ QWFET on Si with the composite buffer described above. The use of a combination of wet and RIE etch to recess the gate towards the channel, as well as Pt/Au Schottky gates, enable enhancement-mode (e-mode) operation and improve short channel performance of the device. The $I_D$-$V_{DS}$ characteristics of the e-mode $L_G$=80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 1.3µm composite buffer layer is shown in Fig. 8. Figs. 9a and 9b show the $I_D$-$V_G$ characteristics of the e-mode $L_G$=80nm $In_{0.7}Ga_{0.3}As$ QWFETs on Si with 2µm and 1.3µm buffer, respectively. The Schottky gate leakage is also included for reference. Both devices exhibit good transistor characteristics and high performance at $V_{DS}$=0.5V. The $L_G$=80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 1.3µm composite buffer achieves threshold voltage ($V_T$) = + 0.11V, $I_{Dsat}$ = 0.32mA/µm and $I_{ON}/I_{OFF}$ = 2150 at $V_{DS}$=0.5V with 0.5V $V_G$ swing. Fig. 10 shows $V_T$ as a function of $L_G$ for the e-mode and depletion-mode (d-mode) $In_{0.7}Ga_{0.3}As$ QWFETs on Si. A positive $V_T$ shift of ~600mV from d-mode to e-mode operation was accomplished through gate recess etch. Figs. 11 and 12 show the sub-threshold slope (SS) and drain induced barrier lowering (DIBL), respectively as a function of $L_G$ for $In_{0.7}Ga_{0.3}As$ QWFETs on Si, demonstrating improved SS and DIBL of e-mode over d-mode devices. Fig.13 shows the transconductance ($G_m$) characteristics of e-mode and d-mode $L_G$ =80nm $In_{0.7}Ga_{0.3}As$ QWFETs on Si with different composite buffer thicknesses at $V_{DS}$ = 0.5V. The improved $G_m$'s of the e-mode devices with 1.3µm and 1.5µm buffer layers over that of the e-mode device with 2µm buffer are due to the improved transistor fabrication process. Fig. 14 shows the current gain ($h_{21}$) versus frequency of the e-mode $L_G$=80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 1.3µm composite buffer at $V_{DS}$ = 0.5V. Fig. 15 shows the cut-off frequency as a function of DC power dissipation comparing the e-mode $L_G$=80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 1.5µm composite buffer at $V_{DS}$=0.5V versus the standard $L_G$=60nm Si n-MOSFET transistor at both $V_{DS}$=0.5V and 1.1V. Comparing to the Si n-MOSFET, the e-mode $In_{0.7}Ga_{0.3}As$ QWFET on Si exhibits >10X reduction in DC power dissipation for the same speed performance or >2X gain in speed performance for the same power.

## Conclusions

$In_{0.7}Ga_{0.3}As$ quantum well structure has been successfully integrated onto Si substrate using a novel, thin composite metamorphic buffer architecture with total buffer thickness scaled down to 1.3µm, resulting in high-performance short-channel enhancement-mode $In_{0.7}Ga_{0.3}As$ QWFETs on Si substrate with good device characteristics for future high-speed, ultra-low power digital logic applications.

## References


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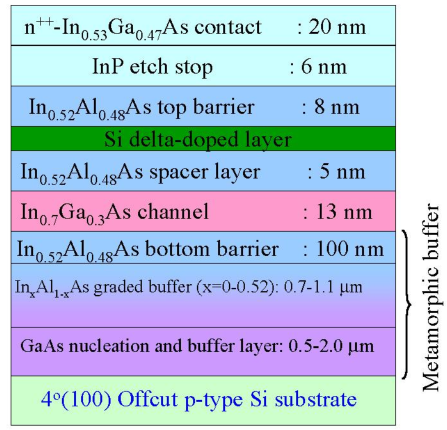


**Fig.1**: Heterogeneous integration of $In_{0.7}Ga_{0.3}As$ QWFETs on Si using metamorphic composite buffer architecture consisting of GaAs and $In_xAl_{1-x}As$ graded buffer layers. The composite buffer in this work has total thickness in the range of 1.3µm to 3.2µm.

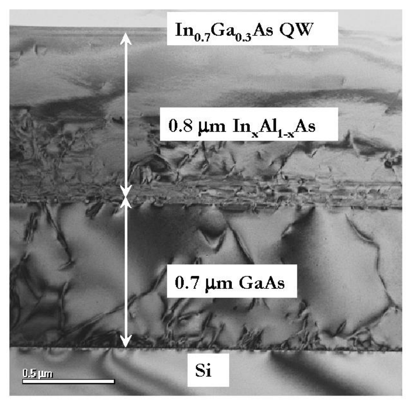


**Fig. 2a**: Cross-sectional TEM image of $In_{0.7}Ga_{0.3}As$ QWFET on Si using 1.5µm composite buffer. The misfit and threading dislocations are predominantly contained in the composite buffer, with the $In_{0.7}Ga_{0.3}As$ QW virtually defect-free.

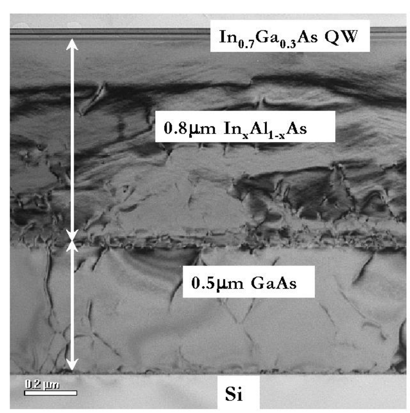


**Fig. 2b**: Cross-sectional TEM image of $In_{0.7}Ga_{0.3}As$ QWFET on Si using composite buffer with total thickness of 1.3µm. The active $In_{0.7}Ga_{0.3}As$ QW is virtually defect-free.

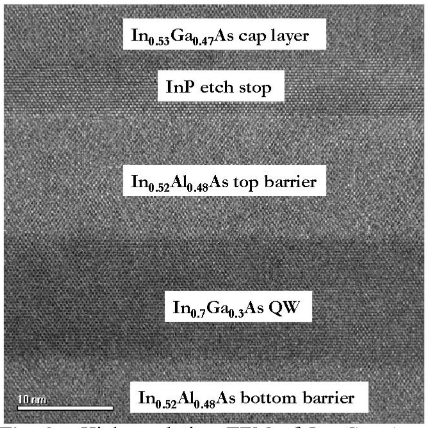


**Fig. 2c**: High-resolution TEM of $In_{0.7}Ga_{0.3}As$ QW, $In_{0.52}Al_{0.48}As$ barriers, InP etch stop and $In_{0.53}Ga_{0.47}As$ cap layer. The device layers are defect-free.

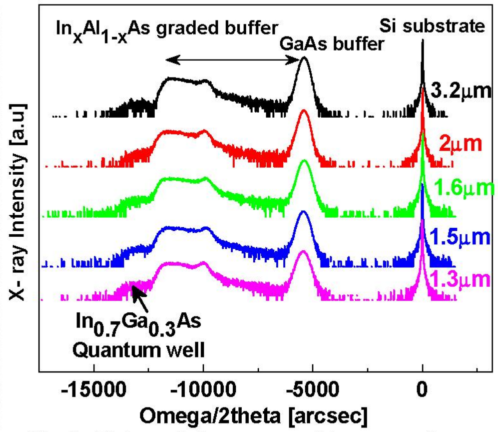


**Fig. 3**: High-resolution x-ray rocking curves from the (004) Bragg lines of $In_{0.7}Ga_{0.3}As$ QWFET structures on Si substrates with different composite buffer thicknesses ranging from 1.3-3.2μm.

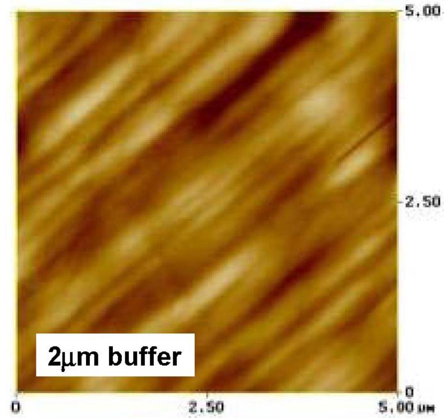


**Fig. 4a**: AFM image from the surface of $In_{0.7}Ga_{0.3}As$ QW layer on Si with 2μm composite buffer shows cross-hatch pattern with surface *rms* roughness of 30Å.

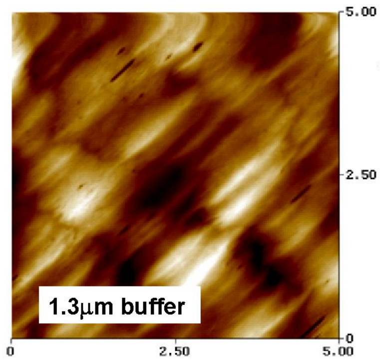


**Fig. 4b**: AFM image from the surface of $In_{0.7}Ga_{0.3}As$ QW layer on Si with 1.3μm composite buffer shows cross-hatch pattern with surface *rms* roughness of 39Å.

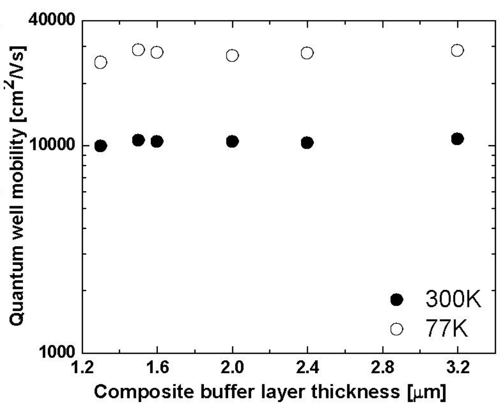


**Fig. 5a**: $In_{0.7}Ga_{0.3}As$ QW electron mobility versus composite buffer layer thickness on Si at 300K and 77K. No mobility degradation is observed, demonstrating that the metamorphic buffer architecture is effective in filtering dislocations.

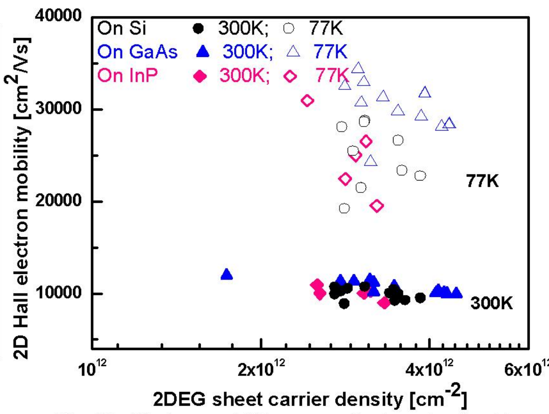


**Fig. 5b**: Electron mobility versus sheet carrier density ($N_s$) in $In_{0.7}Ga_{0.3}As$ QW grown on Si (via novel composite buffer), GaAs and InP substrates at 300K and 77K. No degradation in QW mobility on Si despite >8% lattice mismatch, demonstrating effective dislocation filtering with the composite metamorphic buffer architecture on Si.

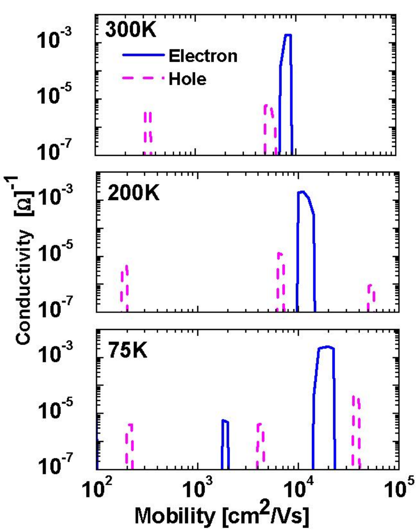


**Fig. 6a**: QMSA mobility spectra for $In_{0.7}Ga_{0.3}As$ QW on Si at different temperature demonstrating no parallel, parasitic conduction to the active $In_{0.7}Ga_{0.3}As$ channel.

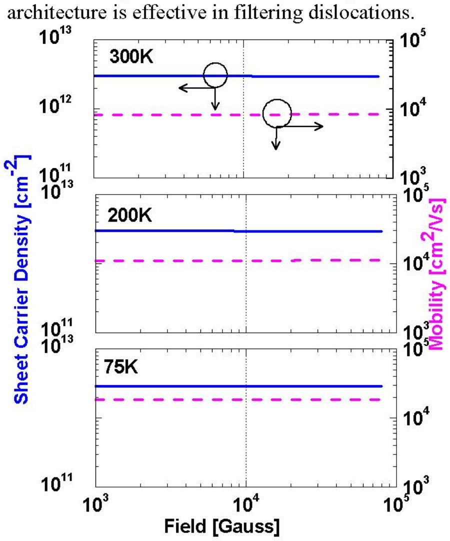


**Fig. 6b**: Sheet carrier density ($N_s$) and electron mobility show no dependence on magnetic field at different temp, indicating no parallel, parasitic conduction in the composite buffer layer on Si.

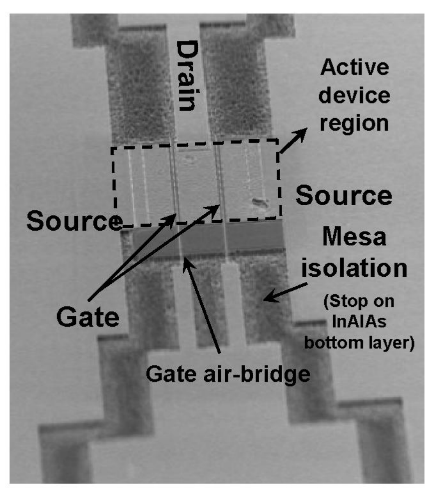


**Fig.7**: SEM micrograph of a two-finger $In_{0.7}Ga_{0.3}As$ QWFET on Si with Pt/Au gate air-bridge at the mesa edge and Ti/Pt/Au source/drain metals.

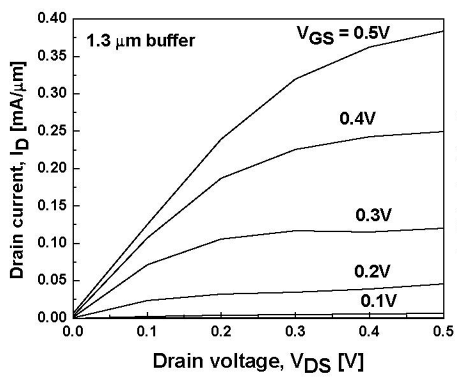


**Fig.8**: $I_D$-$V_{DS}$ characteristics of enhancement-mode $L_G$=80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 1.3μm composite buffer at room temperature.

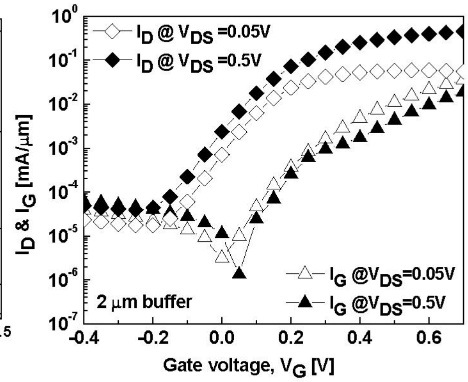


**Fig. 9a**: Drain current ($I_D$) and gate leakage ($I_G$) versus $V_G$ of enhancement-mode $L_G$=80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 2μm composite buffer at room temperature. $V_T$ = + 0.07V, $I_{Dsat}$ = 0.25mA/μm, $I_{ON}/I_{OFF}$ = 2500 at $V_{DS}$=0.5V with 0.5V $V_G$ swing.

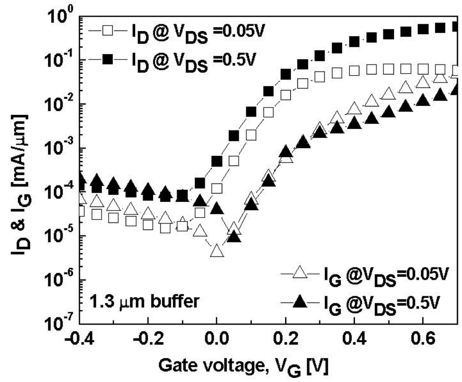


**Fig. 9b**: Drain current ($I_D$) and gate leakage ($I_G$) versus $V_G$ of enhancement-mode $L_G$=80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 1.3μm composite buffer at room temperature. $V_T$ = +0.11V, $I_{Dsat}$ = 0.32mA/μm, $I_{ON}/I_{OFF}$ = 2150 at $V_{DS}$=0.5V with 0.5V $V_G$ swing.

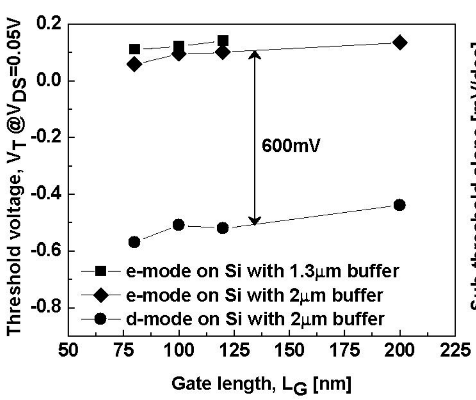


**Fig. 10**: Threshold voltage ($V_T$) as a function of $L_G$ for enhancement-mode (e-mode) and depletion-mode (d-mode) $In_{0.7}Ga_{0.3}As$ QWFETs on Si. Positive $V_T$ shift of about 600mV from d-mode operation to e-mode operation was accomplished through gate recess etch.

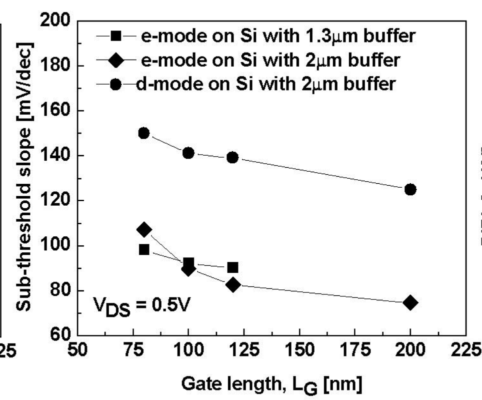


**Fig. 11**: Sub-threshold slope (SS) as a function of $L_G$ for e-mode and d-mode $In_{0.7}Ga_{0.3}As$ QWFETs on Si, showing improved SS of e-mode over d-mode devices due to shorter gate to channel separation in e-mode.

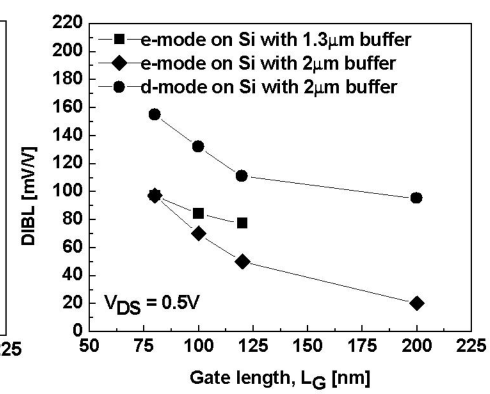


**Fig.12**: DIBL as a function of $L_G$ for e-mode and d-mode $In_{0.7}Ga_{0.3}As$ QWFETs on Si, showing improved DIBL of e-mode devices over d-mode due to shorter gate to channel separation in e-mode.

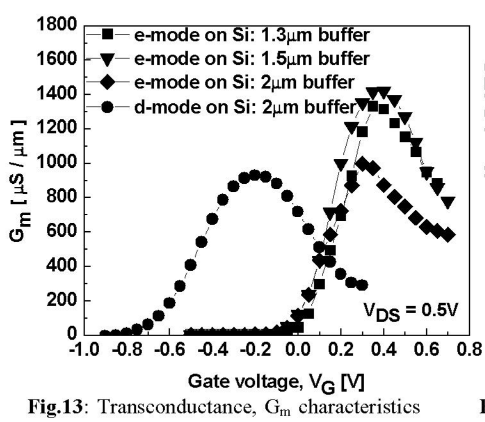


**Fig.13**: Transconductance, $G_m$ characteristics of e-mode and d-mode $L_G$ =80nm $In_{0.7}Ga_{0.3}As$ QWFETs on Si with different composite buffer thicknesses at $V_{DS}$ = 0.5V.

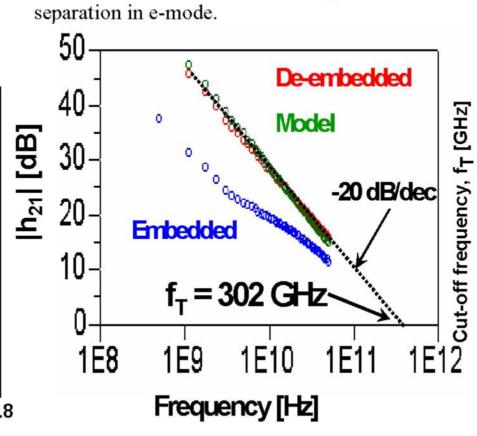


**Fig. 14**: Current gain ($h_{21}$) versus frequency for the 80nm $L_G$ enhancement-mode $In_{0.7}Ga_{0.3}As$ QWFET on Si with 1.3μm composite buffer, showing the embedded and de-embedded data at $V_{DS}$ = 0.5V.

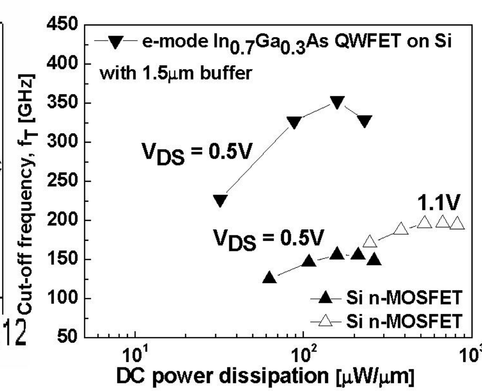


**Fig. 15**: Cut-off frequency as a function of DC power dissipation for the enhancement-mode $L_G$=80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 1.5μm composite buffer at $V_{DS}$=0.5V, versus standard Si n-MOSFET transistor with $L_G$ = 60nm at $V_{DS}$=0.5V and 1.1V.